REMARKS/ARGUMENTS

The Office Action mailed June 28, 2005 has been received and reviewed. Claims 19, 21 through 23, and 25 through 34 are currently pending in the application. Claims 19, 21 through 23, 25, 27, and 29 through 34 stand rejected. Claims 26 and 28 have been objected to as being dependent upon rejected base claims, but the indication of allowable subject matter in such claims is noted with appreciation. Applicant has amended claim 34 and respectfully requests reconsideration of the application in light of the arguments set forth hereinbelow.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Japanese Patent No. JP 63-179537 to Yasuhide et al. in View of U.S. Patent No. 5,279,991 to Minahan et al. and Further in View of U.S. Patent No. 5,281,846 to Kaiser

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yasuhide et al. (Japanese Patent No. JP 63-179537) in view of Minahan et al. (U.S. Patent No. 5,279,991), and further in view of Kaiser (U.S. Patent No. 5,281,846). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 19 is improper because the prior art references do not teach or suggest all the claim limitations. In particular, none of the prior art references teach or suggest "electrically grounding a base die via the layer of electrically conductive epoxy adhesive and the at least one stack die," as recited in claim 19.

The limited portions of Yasuhide et al. set forth in the English language, together with the figures provided therein, teach a method of mounting a semiconductor device in which a first semiconductor device is mounted face-down on a circuit board. A second semiconductor device is then mounted face-up on top of the first semiconductor device. The second semiconductor device is then wire bonded to the circuit board.

It is evident that the integrated circuit of the first semiconductor device and the integrated circuit of the second semiconductor device taught by Yasuhide et al. each electrically communicate with conductive lands on the surface of the circuit board. Yasuhide et al., however, does not teach electrically conductive adhesive. Furthermore, Yasuhide et al. does not teach how either of the semiconductor devices are electrically grounded, and does not teach or suggest grounding the first semiconductor device through the second conductor device by way of electrically conductive epoxy adhesive provided between the first semiconductor device and the second semiconductor device.

Minahan et al. teaches a method for fabricating stacks of semiconductor devices in which a curable adhesive may be used to attach individual semiconductor devices together. Minahan et al., column 4, lines 12-13, 34-37. Minahan et al., however, does not teach electrically conductive adhesive. Furthermore, Minahan et al. does not teach how the semiconductor devices described therein are electrically grounded, and does not teach or suggest grounding a base semiconductor device through another semiconductor device that is mounted thereon by way of electrically conductive epoxy adhesive between the base semiconductor device and the semiconductor device mounted thereon.

Kaiser teaches an electronic component that includes a semiconductor chip mounted on a surface of a flat capacitor with electrically conductive adhesive. Kaiser, column 2, lines 41-61. Kaiser does not teach any other semiconductor chip mounted on the first semiconductor chip. Furthermore, Kaiser does not teach how the semiconductor chip described therein is electrically grounded, and does not teach or suggest grounding the semiconductor chip through another semiconductor chip that is mounted thereon by way of electrically conductive adhesive. Nor does it teach or suggest grounding the semiconductor chip by way of the capacitor to which it is attached.

Moreover, Applicant submits one of ordinary skill in the art would not be motivated to modify the Kaiser device so as to provide grounding of the semiconductor device through the capacitor. Such a modification would likely result in the Kaiser device not functioning in the manner as described thereby. For example, if the semiconductor device were grounded by way of the capacitor, Applicant submits that such grounding would likely result in the capacitor not holding the charge as desired and designed. In other words, such a configuration would likely result in the shorting out of the capacitor. Thus, any such modification would likely result in the Kaiser device becoming inoperable or, at the very least, inadequate for its intended purpose.

As none of the cited references teach or suggest grounding a semiconductor die by way of a layer of electrically conductive epoxy adhesive and another semiconductor die stacked thereon, Applicant respectfully asserts that the prior art references do not teach or suggest all the claim limitations. For this reason, Applicant respectfully requests that the Examiner withdraw the rejection of independent claim 19 under 35 U.S.C. § 103(a).

Obviousness Rejection Based on Japanese Patent No. JP 63-179537 to Yasuhide et al. and U.S. Patent No. 5,279,991 to Minahan et al. in View of U.S. Patent No. 5,281,846 to Kaiser and Further in View of U.S. Patent No. 5,323,060 to Fogal et al.

Claims 21 through 23, 25, 27, 29, and 33 through 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yasuhide et al. (Japanese Patent No. JP 63-179537) and Minahan et al. (U.S. Patent No. 5,279,991) in view of Kaiser (U.S. Patent No. 5,281,846) and further in view of Fogal et al. (U.S. Patent No. 5,323,060). Applicant respectfully traverses this rejection, as hereinafter set forth.

The 35 U.S.C. § 103(a) obviousness rejections of claims 21 through 23, 25, 27, 29, and 33 through 34 are improper because the prior art references do not teach or suggest all the claim limitations. In particular, none of the prior art references teach or suggest "electrically grounding a base die via the layer of electrically conductive epoxy adhesive and the at least one stack die," as recited in claim 19, from which each of claims 21 through 23, 25, 27, 29, and 33 through 34 depends (either directly or indirectly).

As set forth above, Yasuhide et al., Minahan et al., and Kaiser do not teach or suggest grounding a semiconductor die by way of a layer of electrically conductive epoxy adhesive and another semiconductor die stacked thereon.

Fogal et al. teaches multi-chip modules that include stacked semiconductor chips. Each module includes a base semiconductor chip mounted face-up on a substrate. Fogal et al., column 2, lines 31-38. A second semiconductor chip is mounted face-up on the base semiconductor chip with adhesive disposed therebetween. Fogal et al., column 2, lines 44-51. Fogal et al. also teaches discrete electronic components that are mounted by adhesive on a multi-chip module substrate. Fogal et al., column 3, lines 52-55.

Fogal et al. does not teach how the semiconductor chips described therein are electrically grounded, and certainly does not teach or suggest grounding the base semiconductor chip through another semiconductor chip that is mounted thereon by way of electrically conductive adhesive, as recited in independent claim 19.

Each of dependent claims 21 through 23, 25, 27, 29, and 33 through 34 depends either directly or indirectly from independent claim 19, and includes the limitations recited in claim 19.

As none of the cited references teach or suggest grounding a semiconductor die by way of a layer of electrically conductive epoxy adhesive and another semiconductor die stacked thereon, Applicant respectfully asserts that the prior art references do not teach or suggest all the claim limitations. For this reason, Applicant respectfully requests that the Examiner withdraw the rejection of dependent claims 21 through 23, 25, 27, 29, and 33 through 34 under 35 U.S.C. § 103(a).

Regarding claim 21, Applicant respectfully asserts that none of the prior art references teach or suggest "extending a die-to-component bond wire between the at least one **stack die** and the at least one discrete component," as recited therein. Therefore, Applicant respectfully requests that the Examiner withdraw the rejection of dependent claim 21 under 35 U.S.C. § 103(a) for this additional reason.

Regarding claim 33, Applicant respectfully asserts that none of the prior art references teach or suggest "extending a die-to-component bond wire between the at least one **stack die** and the at least one discrete component," as recited therein. Therefore, Applicant respectfully

requests that the Examiner withdraw the rejection of dependent claim 33 under 35 U.S.C. § 103(a) for this additional reason.

Obviousness Rejection Based on Japanese Patent No. JP 63-179537 to Yasuhide et al. and U.S. Patent No. 5,279,991 to Minahan et al. in View of U.S. Patent No. 5,281,846 to Kaiser and Further in View of U.S. Patent No. 5,399,898 to Rostoker

Claims 30 through 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yasuhide et al. (Japanese Patent No. JP 63-179537) and Minahan et al. (U.S. Patent No. 5,279,991) in view of Kaiser (U.S. Patent No. 5,281,846) and further in view of Rostoker (U.S. Patent No. 5,399,898). Applicant respectfully traverses this rejection, as hereinafter set forth.

The 35 U.S.C. § 103(a) obviousness rejections of claims 30 through 32 are improper because the prior art references do not teach or suggest all the claim limitations. In particular, none of the prior art references teach or suggest "electrically grounding a base die via the layer of electrically conductive epoxy adhesive and the at least one stack die," as recited in claim 19, from which each of claims 30 through 32 depends (either directly or indirectly).

As set forth above, Yasuhide et al., Minahan et al., and Kaiser do not teach grounding a semiconductor die by way of a layer of electrically conductive epoxy adhesive and another semiconductor die stacked thereon.

Rostoker teaches multi-chip assemblies that include multiple semiconductor dice that are stacked in a "limited-overlap" configuration. Rostoker, column 15, lines 5-7. The semiconductor dice used in the assemblies can include conductive bumps formed on both major surfaces of each die. Rostoker, column 10, lines 17-22.

Rostoker does teach with reference to FIG. 2b that "[i]n a typical integrated circuit die application, the substrate material 226 should be grounded or held at a constant potential. Openings 223a and 223b formed in insulating layer 225b provide access to substrate material 226. Bump contacts 222a and 222b are disposed on the bottom surface 224b over holes 223a and 223b, respectively, such that they make electrical contact with substrate material 226." Rostoker, column 11, lines 31-38.

Rostoker does not teach or suggest grounding a base semiconductor chip through another semiconductor chip that is mounted thereon by way of electrically conductive adhesive, as recited

in independent claim 19, from which each of dependent claims 30 through 32 depends either directly or indirectly.

As none of the cited references teach grounding a semiconductor die by way of a layer of electrically conductive epoxy adhesive and another semiconductor die stacked thereon, Applicant respectfully asserts that the prior art references do not teach or suggest all the limitations of any one of claims 30 through 32. For this reason, Applicant respectfully requests that the Examiner withdraw the rejection of dependent claims 30 through 32 under 35 U.S.C. § 103(a).

Objections to Claims 26 and 28/Allowable Subject Matter

Claims 26 and 28 stand objected to as being dependent upon rejected base claims, but are indicated to contain allowable subject matter and would be allowable if placed in appropriate independent form. The indication of allowable subject matter in such claims is noted with appreciation. Applicants submit that claim 19, from which claims 26 and 28 depend, is in condition for allowance and, therefore, claims 26 and 28 are in condition for allowance.

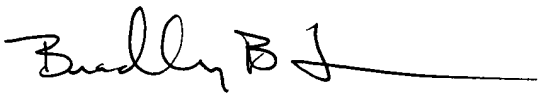
ENTRY OF AMENDMENTS

The amendments to claim 34 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 19, 21 through 23, and 25 through 34 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



Bradley B. Jensen
Registration No. 46,801
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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